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01_Revision_History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1.1	RC00	2015-03	GW	- Initial design	
2.0	RC00	2021-02	GF	- Bug fixes, new capacitor values	
2.2	RC00	2021-07	GF	- Restored GND plane for better dI/dt immunity	
2.3	RC00	2021-10	GF	- Introduced LDO for better supply stability.	

TLE4972 3ph. vertical pcb

Default_Assembly

2.3

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Siemensstraße 2, 9500 Villach, Austria

10/2021

Link to Top Level Document

02 Top Level
02_Top_Level.SchDoc

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Title	TLE4972 3ph. vertical pcb		
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Size: A3	Document Name: 01_Revision_History.SchDoc	Rel.	Rev. 2.3
Date: 12.10.2021	Time: 11:07:32	Author: GF	Sheet of 3

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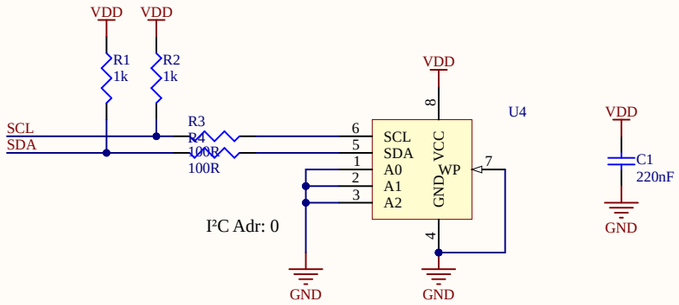
02_Top_Level.SchDoc



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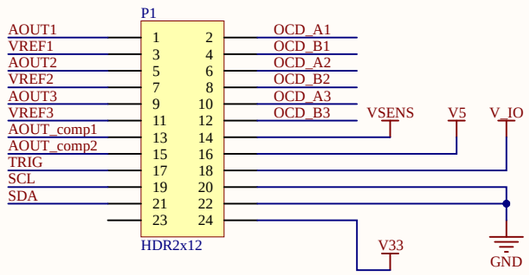

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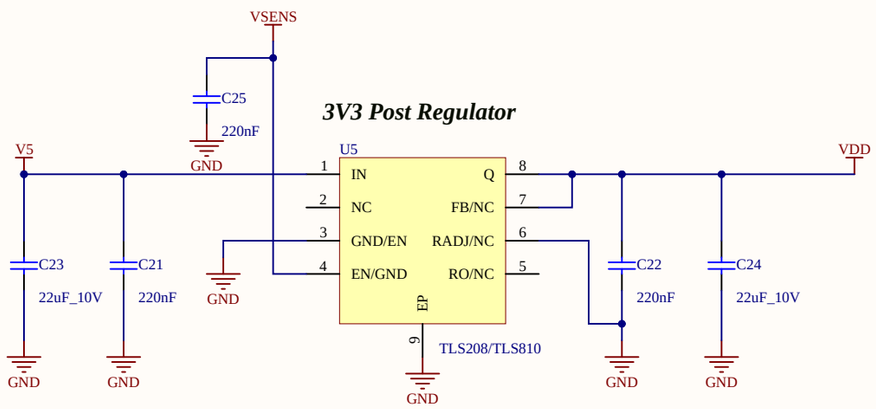

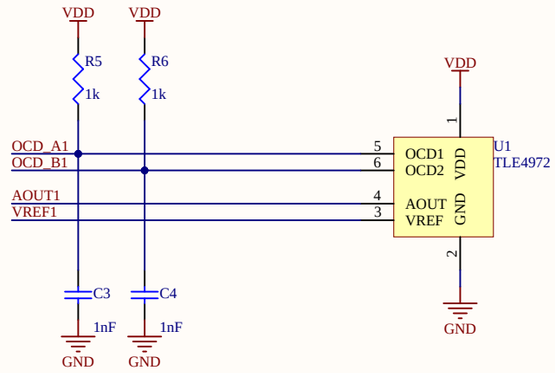

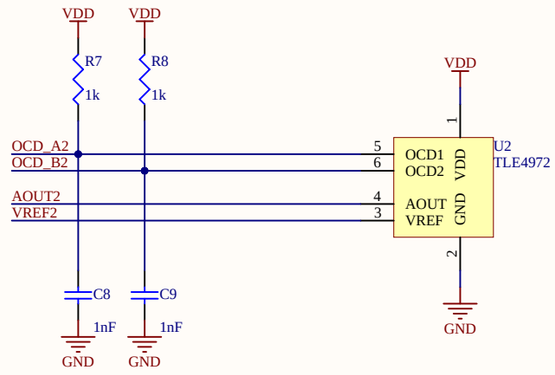

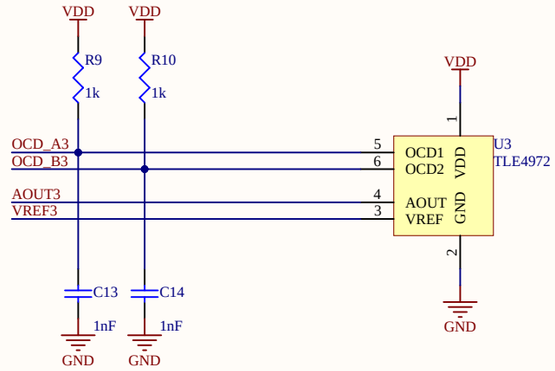

Miscellaneous
Miscellaneous.SchDoc



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Size: A3	Document Name: 02_Top_Level.SchDoc	Rel.	Rev. 2.3
Date: 12.10.2021 Time: 11:07:32	Author: GF	Sheet	of 3

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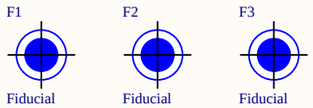
Miscellaneous.SchDoc



BOM Report Configuration



Note!
This component is used to define BOM report configuration.
If this component is deleted before other components from database are placed in this project, the BOM report configuration gets lost!

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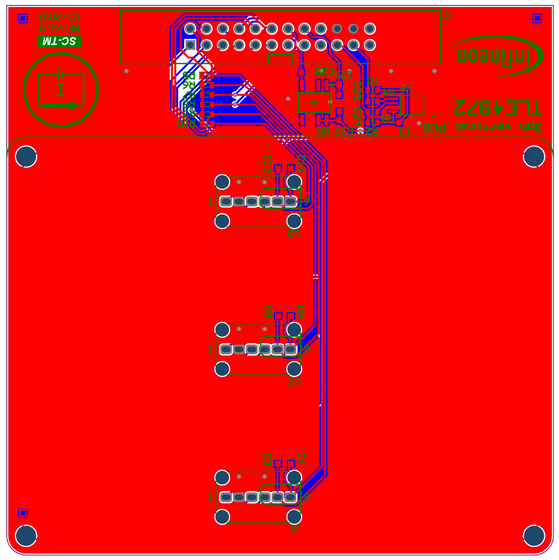

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IFAT DC ATV SC MSS TM
Am Campeon 1–12
85579 NEUBIBERG – GERMANY

Infineon Technologies AG
IFAT DC ATV SC MSS TM
Am Campeon 1–12
81726 MÜNCHEN – GERMANY

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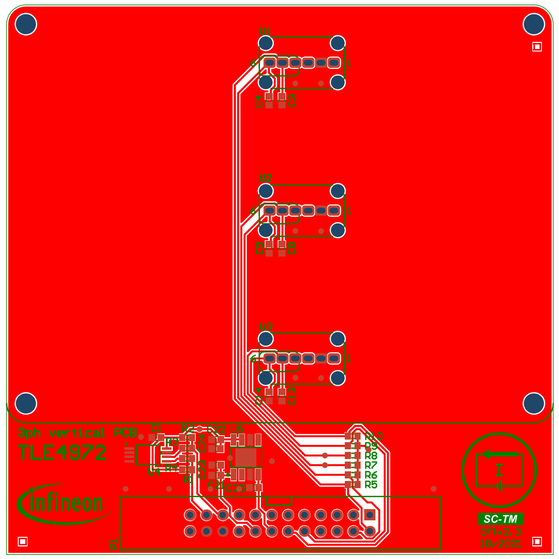

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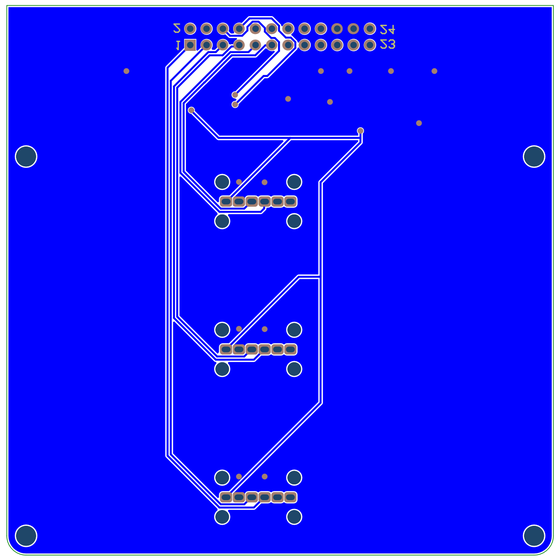

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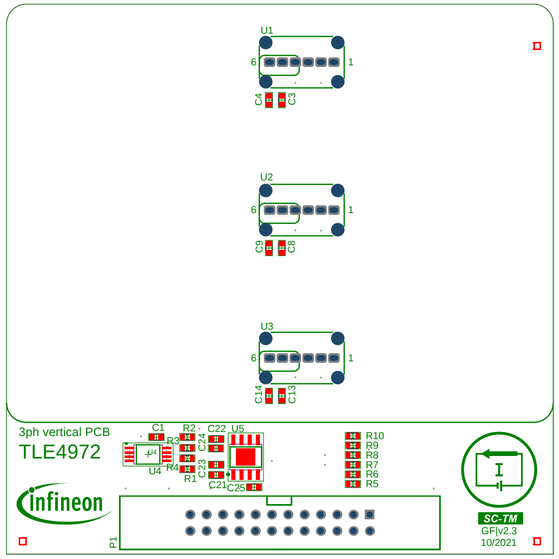

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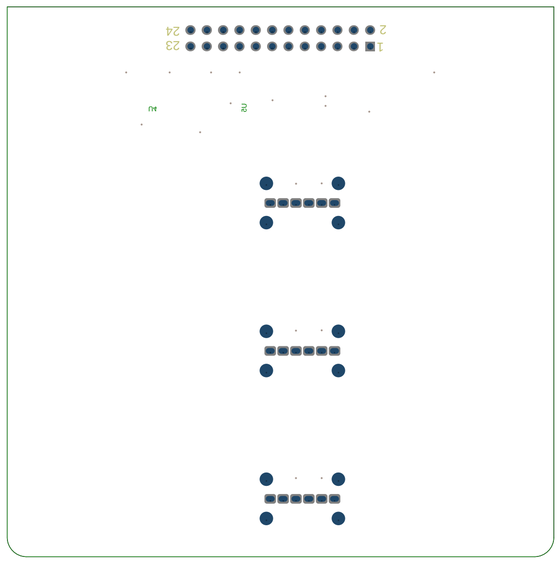

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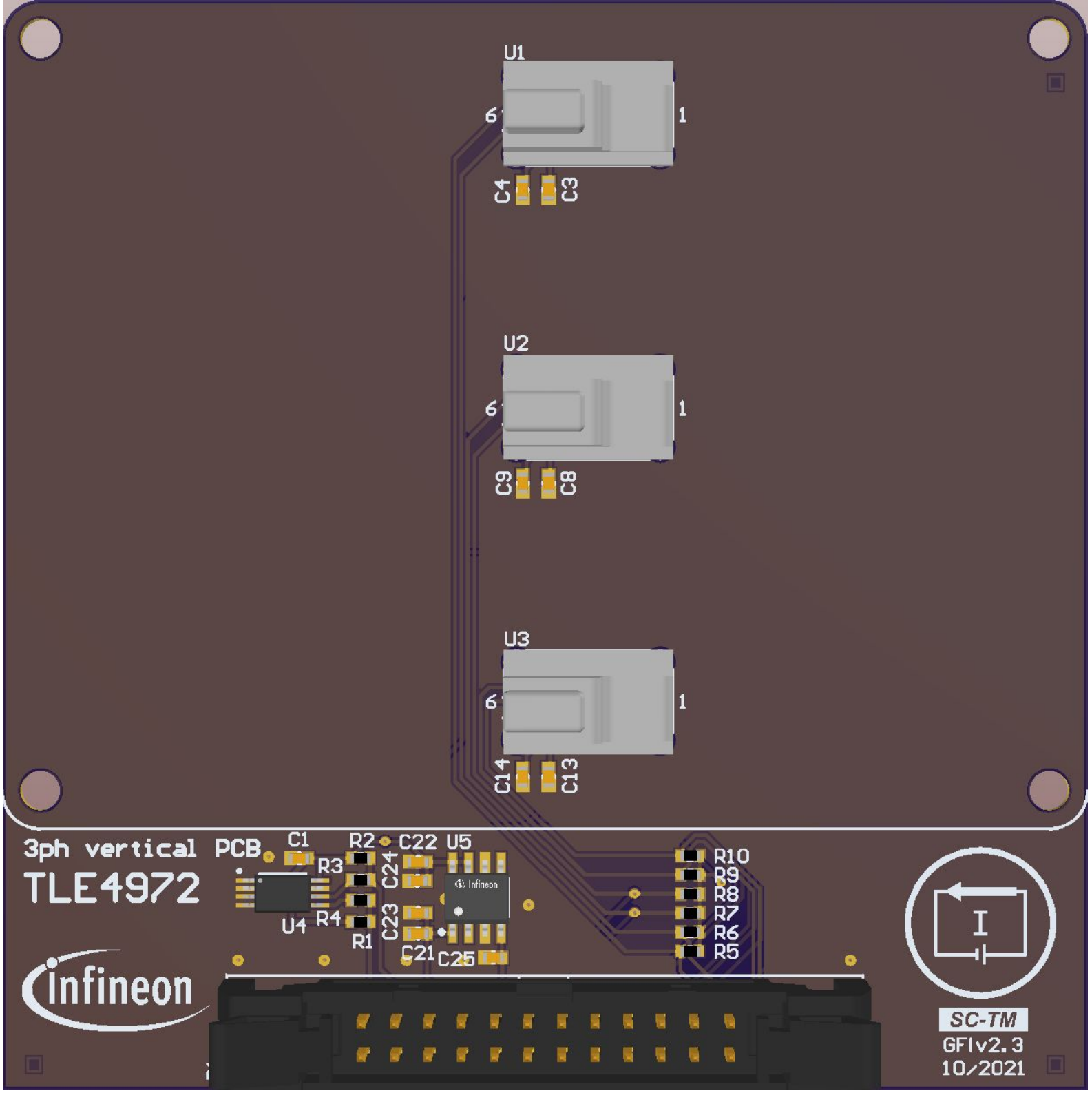
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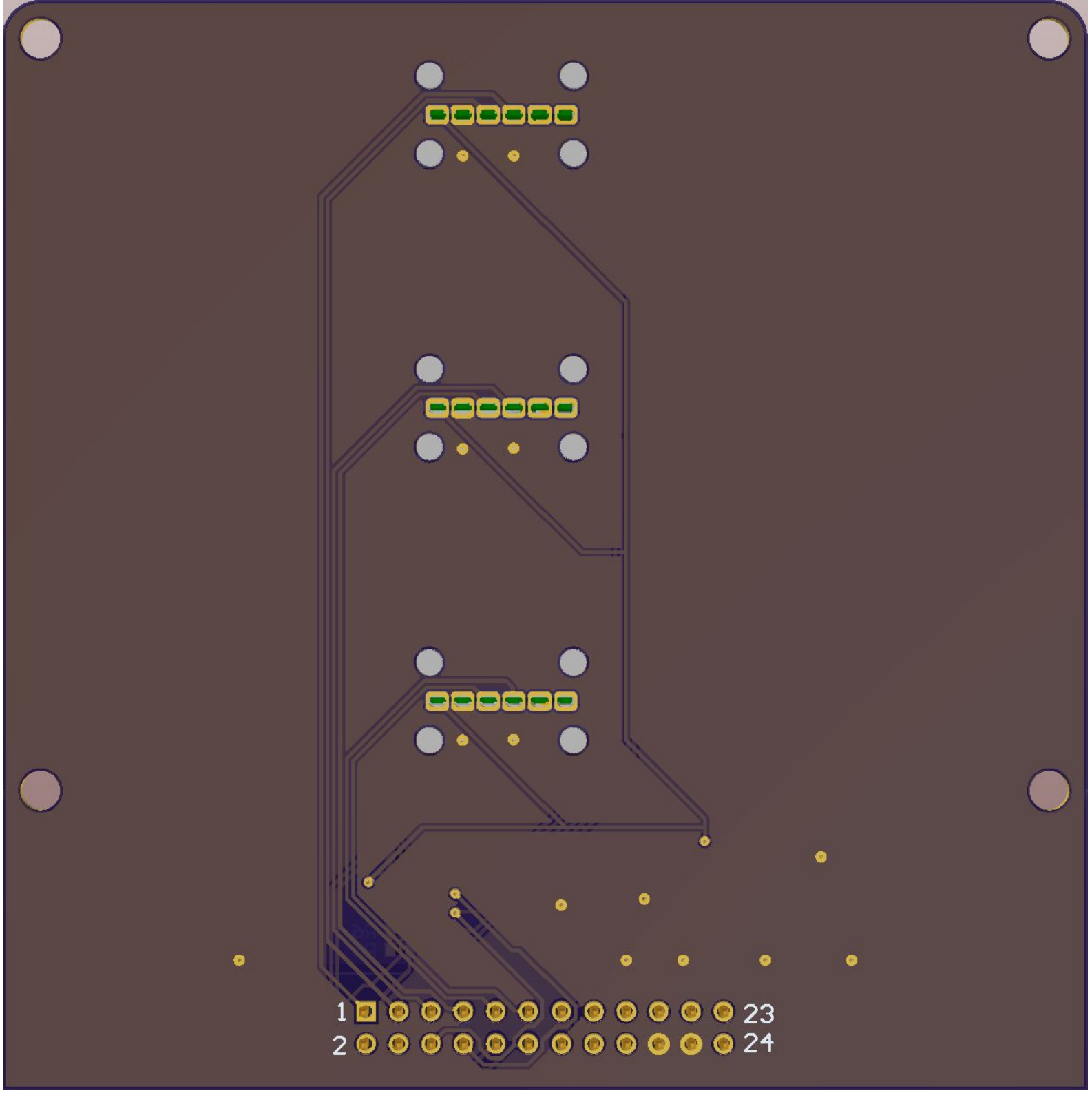
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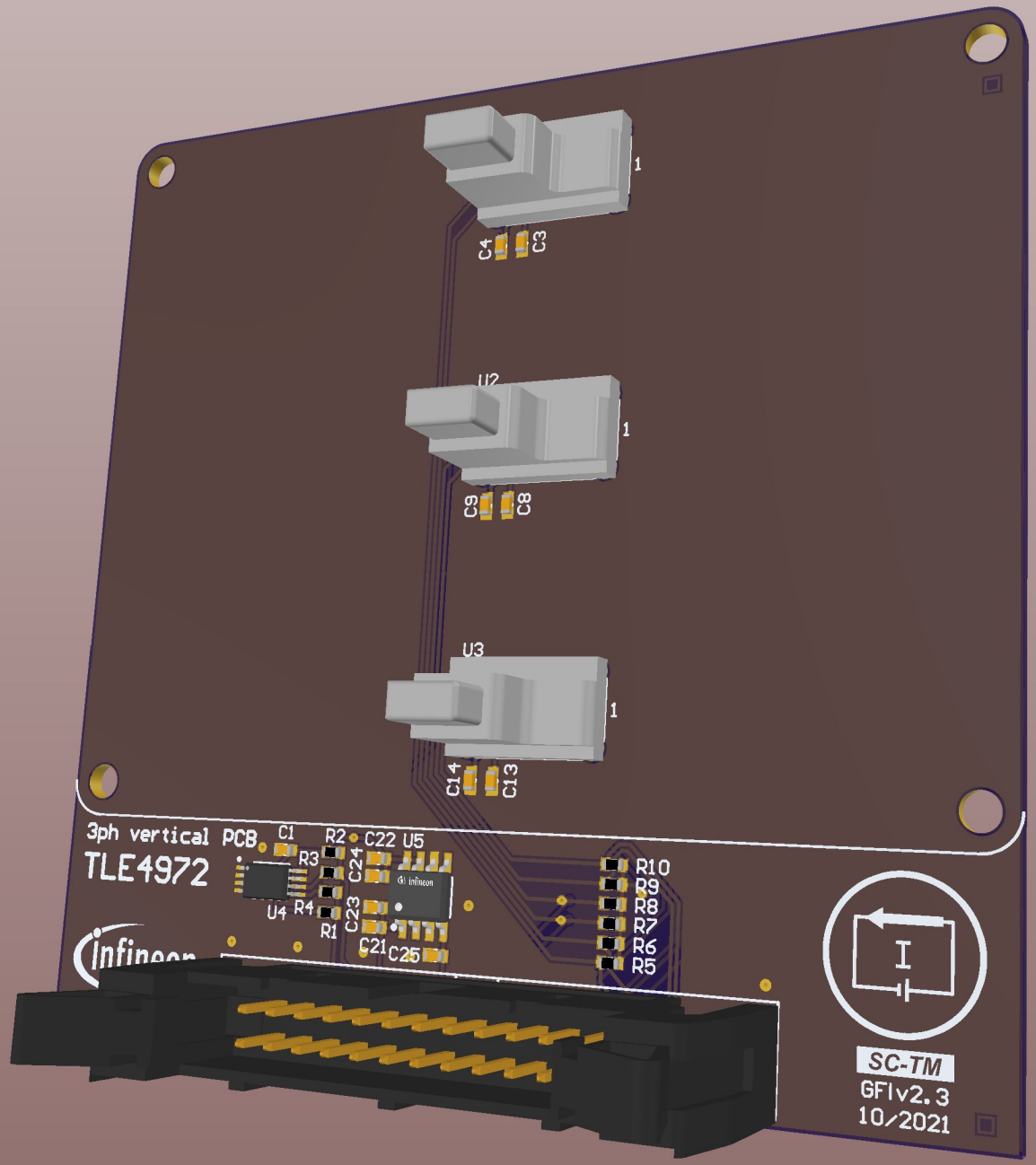
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